IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Marti et al.	Attorney Docket No.: ALTRP0105
Application No.: As Filed Herewith	Examiner: Unassigned
Filed: As Filed Herewith	Group: Unknown

Title: CHIP DEBUGGING INCREMENTAL RECOMPILATION AND REGISTER INSERTION

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on February 09, 2004 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR §1.10, Mailing Label Number EV 333984760 US, addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Ann Lowe

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The non-U.S. references (copies enclosed herewith) listed in the attached PTO Form 1449 may be material to the examination of the above-identified patent application. Applicant submits these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application. Applicant is unable to locate reference number six entitled "Pentium®Processor User's Manual", Vol., 1, Intel®Corporation, 1993; Pgs. 3-11, but believes that the PTO has a copy on file.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure

Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. ALTRP0105).

Respectfully submitted,
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Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. ALTRP0105 Applicant: Marti et al. Filing Date As Filed Herewith	Application No.: As Filed Herewith Group Unknown

U.S. Patent Documents

Examine Initial	No.	Patent No. N	Date	Patentee	Class	Sub-class	Filing Date
	1	4,696,004	09/22/87	Nakajima			
	2	4,788,492	11/29/88	Schubert			
	3	4,835,736	07/11/89	Easterday			
	4	4,847,612	07/11/89	Kaplinsky			
	5	4,873,459	10/10/89	El Gamo et al.			
	6	5,036,473	07/30/91	Butts et al.			
	7	5,058,114	10/15/91	Kuboki et al.			
	8	5,124,588	06/23/92	Baltus et al.			
	9	5,329,470	07/12/94	Sample et al.			
	10	5,365,165	11/15/94	El-Ayat et al.			
	11	5,425,036	06/13/95	Liu et al.			
	12	5,452,231	09/19/95	Butts et al.			
	13	5,568,437	10/22/96	Jamal			
	14	5,572,712	11/05/96	Jamal			
	15	5,629,617	05/13/97	Uhling et al.			
	16	5,640,542	06/17/97	Whitsel et al.			
	17	5,661,662	08/26/97	Butts et al.			
	18	5,717,695	02/10/98	Manela et al.			
	19	5,717,699	02/10/98	Haag et al.			
	20	5,764,079	06/98/98	Patel et al.			
	21	5,821,771	10/13/98	Patel et al.			
	22	5,870,410	02/09/99	Norman et al.			
	23	5,960,191	09/28/99	Sample et al.			
	24	5,983,277	11/09/99	Heile et al.			
	25	6,014,334	01/11/00	Patel et al.			
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	27	6,020,758	02/01/00	Patel et al.			
	28	6,104,211	08/15/00	Alfke			
	29	6,107,821	08/22/00	Kelem et al.			
	30	6,157,210	12/05/00	Zaveri et al.			
	31	6,182,247	01/30/01	Herrmann et al.			
	32	6,212,650	04/03/01	Alfke			

Examine Initial	No.	Patent No. N	Date	Patentee	Class	Sub-class	Filing Date
	33	6,223,148	04/24/01	Stewart et al.			
	34	6,247,147	06/12/01	Beenstra et al.			
	35	6,259,271	07/10/01	Couts-Martin et al.			
	36	6,286,114	09/04/01	Veenstra et al.			
	37	6,317,860	11/13/01	Heile			
	38	6,321,369	11/20/01	Heile et al.			
	39	6,389,558	05/14/02	Herrmann et al.			
	40	6,460,148	01/10/02	Veenstra et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	A	4042262	07/1992	DE				

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	1	Marantz, Joshua, "Enhanced Visibility and Performance in Functional Verification by Reconstruction", Proceedings of the 35th Annual Conference on Design Automation Conference, Pgs. 164-169. 1998.
	2	Stroud, Charles et al., "Evaluation of FPGA Resources for Built-in Self-test of Programmable Logic Blocks", Proceedings of the 1996 ACM 4th International Symposium on Field-programmable Gate Arrays, Pg. 107. 1996.
	3	Collins, Robert R., "Overview of Pentium Probe Mode", (www.x86.org/ariticles/problemd/ProbeMode.htm), August 21, 1998, 3 pgs.
	4	Collins, Robert R., "ICE Mode and the Pentium Processor", (www.x86.org/ddj/Nov97/Nov97.htm), August 21, 1986, 6 Pgs.
	5	"PentiumPro Family Developer's Manual", Volum 1: Specifications, Intel®Corporation, 1996, 9 Pgs.
	6	"Pentium® Processor User's Manual", Volume 1, Intel®Corporation, 1993, Pgs. 3-11.
	7	Xilinx, Inc.; ISE Logic Design Tools: ChipScope

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	8	Synplicity, Inc. "Identify™RTL Debugger" 2003; Pg 1-2.
	9	Altera, "SignalTap Analysis in the Quartus II Software Version 2.0; September 2002, ver. 2.1; Altera Corporation.
	10	Praveen K. Jaini and Nur A. Touba; "Observing Test Response of Embedded Cores through Surround Logic"; 1999 IEEE.
	11	Nur A. Touba and Bahram Pouya; "Testing Embedded Cores Using Partial Isolation Rings"; 1997 IEEE.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.